WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a substrate;

a first semiconductor chip coupled to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

an adhesive layer coupled to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces which are substantially flat in nature; and

an insulator coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.

2. A semiconductor package in accordance with Claim 1 further comprising:

at least one input-output pad being formed on the second surface of the first semiconductor chip; and

at least one first conductive wire connecting the input-output pad of the first semiconductor chip and the substrate.

3. A semiconductor package in accordance with Claim 2 further comprising:

at least one input-output pads formed on the second surface of the second semiconductor chip; and

at least one second conductive wire connecting the input-output pads of the second semiconductor chip and the substrate.

4. A semiconductor package in accordance with Claim 3 wherein the first semiconductor chip is an edge pad type semiconductor chip in which the input-output pad of the first semiconductor chip is formed at an inner circumference of the second surface.

5. A semiconductor package in accordance with Claim 3 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

6. A semiconductor package in accordance with Claim 3 wherein the adhesive layer covers a part of the first conductive wire positioned on the input-output pad of the first semiconductor chip.

7. A semiconductor package in accordance with Claim 3 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

8. A semiconductor package in accordance with Claim 3 wherein a first end of the first conductive wire is bonded on the substrate by ball bonding and a second end of the first conductive wire is bonded on the input-output pad of the first semiconductor chip by stitch bonding.

9. A semiconductor package in accordance with Claim 8 wherein a conductive ball is formed on the input-output pad of the first semiconductor chip bonded by the stitch bonding.

10. A semiconductor package in accordance with Claim 8 further comprising a supporter formed on the first conductive wire connected on the input-output pad so as to support the second semiconductor chip.

11. A semiconductor package in accordance with Claim 3 wherein the first semiconductor chip is a center pad type semiconductor chip in which the input-output pad is formed at the center of the second surface thereof.

12. A semiconductor package in accordance with Claim 3 wherein a first end of the first conductive wire is bonded on the substrate and a second end of the first conductive wire is bonded on the input-output pad of the first semiconductor chip by stitch bonding.

13. A semiconductor package in accordance with Claim 11 wherein a first end of the first conductive wire is bonded on the substrate and a second end of the first conductive wire is bonded on the input-output pad of the first semiconductor chip by stitch bonding.

14. A semiconductor package in accordance with Claim 11 wherein the adhesive layer is a nonconductive liquid phase adhesive.

15. A semiconductor package in accordance with Claim 11 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

16. A semiconductor package in accordance with Claim 3 wherein a section of the first conductive wires is contacted with the insulator.

17. A semiconductor package comprising:

a substrate on which a plurality of circuit patterns is formed;

a first semiconductor chip having first and second surfaces wherein the first surface of the first semiconductor chip is coupled to the substrate,

a plurality of input-output pads formed on the second surface of the first semiconductor chip;

an adhesive layer coupled to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces;

an insulator coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof;

a plurality of input-output pads formed on the second surface thereof;

a plurality of first conductive wires connecting the input-output pads of the first semiconductor chip and the circuit pattern of the substrate;

a plurality of second conductive wires connecting the input-output pads of the second semiconductor chip and the circuit pattern of the substrate; and

a sealing part for sealing the first semiconductor chip, the adhesive layer, the second semiconductor chip, insulator, and the first and the second conductive wires with sealing material.

18. A semiconductor package in accordance with Claim 17 wherein the substrate is one selected from a group consisting of a printed circuit board, a circuit tape, a circuit film, a lead frame, and combinations thereof.

19. A semiconductor package in accordance with Claim 17 further comprising a conductive ball coupled to a surface of the substrate.

20. A semiconductor package in accordance with Claim 17 wherein the substrate has a perforating hole of which size is larger than that of the first semiconductor chip.

21. A semiconductor package comprising:

a substrate;

a first semiconductor chip coupled to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

an adhesive layer coupled to the second surface of the first semiconductor chip; and

a second semiconductor chip having first and second surfaces which are substantially flat in nature; and

means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the means for preventing shorting of wirebonds.

22. A semiconductor package in accordance with Claim 21 further comprising:

at least one input-output pad being formed on the second surface of the first semiconductor chip;

at least one first conductive wire connecting the input-output pad of the first semiconductor chip and the substrate;

at least one input-output pads formed on the second surface of the second semiconductor chip; and

at least one second conductive wire connecting the input-output pads of the second semiconductor chip and the substrate.

23. A method of forming a semiconductor package comprising:

providing a substrate;

coupling a first semiconductor chip to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

laying an adhesive layer to the second surface of the first semiconductor chip; and

providing a second semiconductor chip having first and second surfaces which are substantially flat in nature; and

forming an insulator coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.

24. The method of Claim 23 further comprising:

forming at least one input-output pad on the second surface of the first semiconductor chip; and

coupling at least one first conductive wire from the input-output pad of the first semiconductor chip to the substrate.

25. The method of Claim 23 further comprising:

forming at least one input-output pads on the second surface of the second semiconductor chip; and

connecting at least one second conductive wire from the input-output pads of the second semiconductor chip to the substrate.

26. The method of Claim 23 further comprising:

providing an edge pad type semiconductor chip as the first semiconductor chip; and

forming the input-output pad of the first semiconductor chip at an inner circumference of the second surface.

27. The method of Claim 23 further comprising:

ball bonding a first end of the first conductive wire to the substrate; and

stitch bonding a second end of the first conductive wire to the input-output pad of the first semiconductor chip.

28. The method of Claim 27 further comprising forming a conductive ball on the input-output pad of the first semiconductor chip bonded by the stitch bonding.

29. The method of Claim 27 further comprising forming a supporter on the first conductive wire connected on the input-output pad so as to support the second semiconductor chip.

30. The method of Claim 23 further comprising:

providing a center pad type semiconductor chip as the first semiconductor chip; and

forming the input-output pad at a center of the second surface thereof.

31. The method of Claim 23 further comprising:

bonding a first end of the first conductive wire to the substrate; and

stitch bonding a second end of the first conductive wire to the input-output pad of the first semiconductor chip.

32. The method of Claim 30 further comprising:

bonding a first end of the first conductive wire to the substrate; and

stitch bonding a second end of the first conductive wire to the input-output pad of the first semiconductor chip.

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